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AUTHOR(S):

Noborio, Masato; Suda, Jun; Kimoto, Tsunenobu

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1580-V–40-m$\Omega \cdot$ cm^2 Double-RESURF MOSFETs on 4H-SiC $(000\bar{1})$

Masato Noborio, *Student Member, IEEE*, Jun Suda, and Tsunenobu Kimoto, *Senior Member, IEEE*

***Abstract*—Double-reduced-surface-field (RESURF) MOSFETs with N_2O-grown oxides have been fabricated on the 4H-SiC $(000\bar{1})$ face. The double-RESURF structure is effective in reducing the drift resistance, as well as in increasing the breakdown voltage. In addition, by utilizing the 4H-SiC $(000\bar{1})$ face, the channel mobility can be increased to over 30 cm^2/V $\cdot$ s, and hence, the channel resistance is decreased. As a result, the fabricated MOSFETs on 4H-SiC $(000\bar{1})$ have demonstrated a high breakdown voltage (V_B) of 1580 V and a low on-resistance (R_{ON}) of 40 m$\Omega \cdot$ cm^2. The figure-of-merit (V_B^2/R_{ON}) of the fabricated device has reached 62 MW/cm^2, which is the highest value among any lateral MOSFETs and is more than ten times higher than the "Si limit."**

***Index Terms*—Breakdown voltage, MOSFET, on-resistance, reduced surface field (RESURF), silicon carbide (SiC).**

I. Introduction

SILICON carbide (SiC) has attracted attention as a potential wide-bandgap semiconductor for high-power, high-frequency, and high-temperature devices because of its superior properties [1]. 4H-SiC MOSFET is one of the most promising devices for power electronics used in the foreseeable future [2]. Several groups have addressed the development of SiC vertical power MOSFETs and have already demonstrated the superior characteristics in SiC MOSFETs [3]–[5].

SiC lateral high-voltage MOSFETs are key components of SiC-based power integrated circuits [6] and should be developed. The SiC lateral high-voltage MOSFETs previously reported [6]–[9] have mostly reduced surface field (RESURF) structure [10] to increase the breakdown voltage. For further improvement, the authors' group has proposed a two-zone double RESURF structure [11], which is effective to achieve both high breakdown voltage and low on-resistance. The reported MOSFETs on 4H-SiC (0001) exhibited a breakdown voltage of 1540 V and an on-resistance of 55 m$\Omega \cdot$ cm^2 [12].

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M. Noborio and J. Suda are with the Department of Electronic Science and Engineering, Kyoto University, Kyoto 615-8510, Japan (e-mail: noborio@semicon.kuee.kyoto-u.ac.jp).

T. Kimoto is with the Department of Electronic Science and Engineering, Kyoto University, Kyoto 615-8510, Japan, and also with the Photonics and Electronics Science and Engineering Center, Kyoto University, Kyoto 615-8510, Japan.

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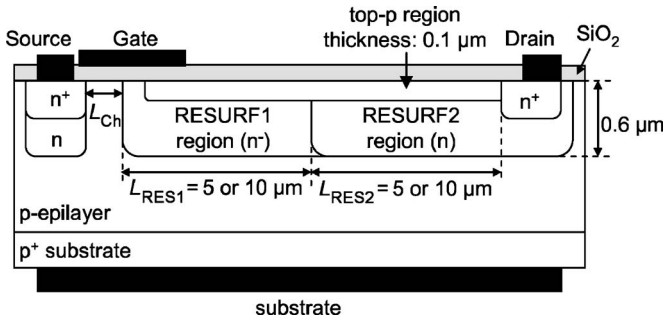

Fig. 1. Schematic structure of a SiC two-zone double-RESURF MOSFET.

In this letter, the authors fabricated the two-zone double-RESURF MOSFETs on 4H-SiC $(000\bar{1})$. By utilizing the 4H-SiC $(000\bar{1})$ face, the channel mobility can be increased [13], leading to a lower on-resistance. The fabricated RESURF MOSFETs exhibit superior characteristics to the lateral MOSFETs previously reported.

II. Device Fabrication

Fig. 1 shows the structure of a two-zone double-RESURF MOSFET. The double RESURF structure has a top-p region placed on the top of the RESURF region [14]. Since the double-RESURF region is depleted not only from the bottom p-epilayer/RESURF junction but also from the RESURF/top-p junction, a higher RESURF dose can be employed than in normal RESURF MOSFETs, leading to a lower on-resistance. To achieve high breakdown voltage, a two-zone RESURF structure [7] was also employed. The fabricated MOSFETs have RESURF1 and RESURF2 lengths of 5 μm each (total drift length: 10 μm) or 10 μm each (total drift length: 20 μm).

Double-RESURF MOSFETs were fabricated on 10-μm-thick p-type 4H-SiC $(000\bar{1})$ epilayers with an acceptor concentration of 6×10^{15} cm^{-3}. The top-p region of double-RESURF MOSFETs was formed by a self-aligned process, and the detail of the fabrication process was described elsewhere [11], [12]. The RESURF1, RESURF2, and top-p doses (D_{RES1}, D_{RES2}, and D_{TP}, respectively) were varied while keeping the same *net* RESURF1 dose $(D_{RES1} - D_{TP})$ of 1×10^{12} cm^{-2} and *net* RESURF2 dose $(D_{RES2} - D_{TP})$ of 9×10^{12} cm^{-2} to achieve high breakdown voltage [11]. Thermal oxidation to form gate oxides was carried out in dry N_2O (10% diluted in N_2) ambient at 1300 °C [15], [16]. The gate oxide thickness (d) was 80 nm. Al was used as the gate electrode. The typical channel length (L_{Ch}) and width (W) of RESURF MOSFETs were 1–5 and

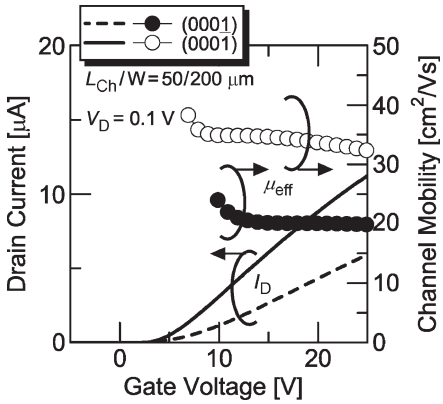

Fig. 2. (Solid line) Gate characteristics and (open circles) the relationship between channel mobility and gate voltage of the $(000\bar{1})$ test MOSFET without a RESURF region, processed on the same wafer, in the linear region (V_D = 0.1 V). The characteristics of a (0001) MOSFET are also shown as the dashed line and closed circles. The solid and dashed lines denote the drain current (I_D), and the closed and open circles mean the effective mobility (μ_{eff}).

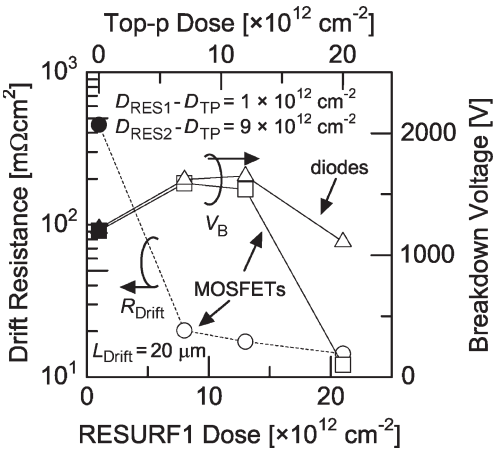

Fig. 3. RESURF1 dose dependence of drift resistance and breakdown voltage for the fabricated 4H-SiC RESURF MOSFETs with a drift length of 20 μm. The open and closed circles represent the drift resistance, the open and closed triangles denote the breakdown voltage for the diodes, and the open and closed boxes indicate the breakdown voltage for the MOSFETs. The closed symbols mean the characteristics of single-RESURF MOSFETs, and the open symbols represent those of double-RESURF MOSFETs.

200 μm, respectively. Test elementary group (TEG) devices to measure the drift resistance and RESURF diodes to evaluate the ideal breakdown voltage [11] were also fabricated on the same wafer.

III. Results and Discussion

Fig. 2 shows the gate characteristics of a 4H-SiC $(000\bar{1})$ test MOSFET without a RESURF region processed on the same wafer of the RESURF MOSFETs. The channel mobility is also shown in Fig. 2. For comparison, the gate characteristics and the gate voltage dependence of the channel mobility for the (0001) MOSFETs are also indicated as the dashed line and closed circles, respectively. The test MOSFET with a N_2O-grown oxide on the 4H-SiC $(000\bar{1})$ face exhibits a threshold voltage of 4.9 V and a high channel mobility of 32–36 $\text{cm}^2/\text{V}\cdot\text{s}$. On the other hand, a high threshold voltage of 7.1 V and a relatively low channel mobility of 21 $\text{cm}^2/\text{V}\cdot\text{s}$ are obtained in the (0001) MOSFET with N_2O-grown oxides. The low threshold voltage in the $(000\bar{1})$ MOSFETs indicates the low density of effective fixed charges, which is attributed to the low interface state density [16]. The $(000\bar{1})$ MOSFETs show 1.5 times higher channel mobility than the (0001) MOSFETs. The high channel mobility naturally reduces the channel resistance.

Fig. 3 shows the relationship between the drift resistance and RESURF1 dose for the double-RESURF MOSFETs with a drift length of 20 μm. The RESURF1 dose dependences of the breakdown voltage for MOSFETs and diodes are also shown. The drift resistance is calculated from the characteristics of the TEG devices with the same doses as the RESURF MOSFETs. The MOSFET with a RESURF1 dose of 1×10^{12} cm^{-2} has a single RESURF structure (without a top-p region, denoted by closed symbols). The drift resistance is reduced to below 25 $\text{m}\Omega\cdot\text{cm}^2$ in the MOSFETs with a long-drift region by increasing the RESURF doses, which agrees with the concept of double RESURF structure. The breakdown voltage was increased to over 1.5 kV by increasing the RESURF1 dose, as far as the RESURF1 dose is kept below 13×10^{12} cm^{-2}, because the electric field crowding at the both gate and drain edges can be relaxed [11]. The breakdown voltage of the RESURF MOSFETs is almost the same as that of the RESURF diodes, which indicates that the MOSFETs broke down in SiC (not in the gate oxides). When the RESURF1 dose was increased to 21×10^{12} cm^{-2}, the RESURF MOSFETs exhibited the reduced breakdown voltage below 500 V, although the RESURF diodes showed a high breakdown voltage over 1 kV. From the device simulation, electric field crowding occurred at the gate oxides near the channel region [12]. In addition, the MOSFETs with high RESURF doses showed destructive breakdown with the considerable increase in gate leakage. These results indicate that the gate oxides break down in the MOSFETs with high RESURF doses. In the case of the MOSFETs with a short drift length, the drift resistance was decreased to below 15 $\text{m}\Omega\cdot\text{cm}^2$ (not shown). In terms of breakdown voltage, the MOSFETs with a short drift region show lower breakdown voltage than the diodes (not shown), as is the case for the double-RESURF MOSFETs on the 4H-SiC (0001) face [11]. This result indicates that the breakdown occurred at the gate oxides (not in SiC). In fact, the MOSFETs with a short drift region showed destructive breakdown.

Fig. 4 shows the output characteristics of the 4H-SiC $(000\bar{1})$ two-zone double-RESURF MOSFET with a long drift length of 20 μm. The MOSFET has a RESURF1 dose of 8×10^{12} cm^{-2}, a RESURF2 dose of 16×10^{12} cm^{-2}, and a top-p dose of 7×10^{12} cm^{-2}. The MOSFET exhibits a threshold voltage of 2.8 V, a low on-resistance of 40 $\text{m}\Omega\cdot\text{cm}^2$ at a gate oxide field of 3 MV/cm, and a high breakdown voltage of 1580 V at zero gate bias. In the calculation of the on-resistance, the cell pitch was assumed to be 27.7 μm, which is equal to the sum of the channel length (1.7 μm), the RESURF length (20 μm), and the source/drain pad length (6 μm). The channel resistance is reduced to 12 $\text{m}\Omega\cdot\text{cm}^2$ in the $(000\bar{1})$ MOSFET. The component of the contact resistance is relatively large (8 $\text{m}\Omega\cdot\text{cm}^2$) because of the nonoptimized process to form the source/drain contact. In the case of the short drift length, the

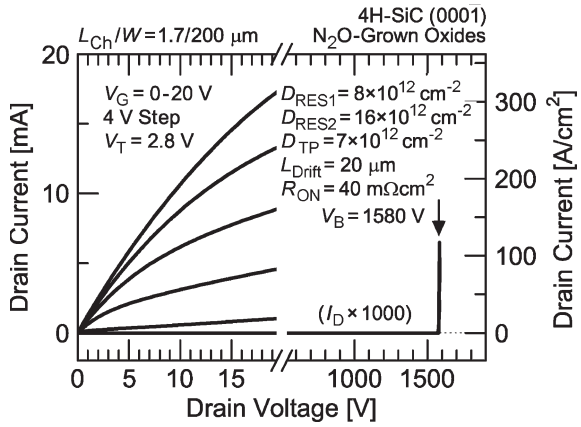

Fig. 4. Output characteristics of a fabricated 4H-SiC $(000\bar{1})$ two-zone double-RESURF MOSFET with a long drift length of 20 μm.

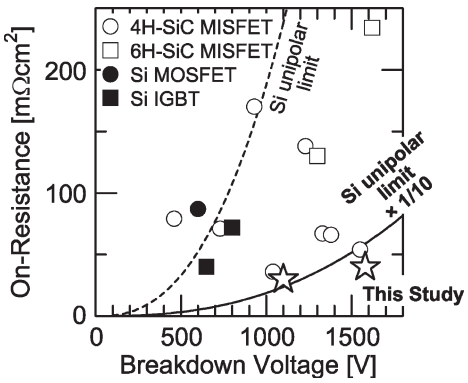

Fig. 5. Breakdown voltage versus on-resistance relationship for major lateral SiC MOSFETs in the literature and in this letter. For comparison, the characteristics of Si lateral MOSFETs and Si lateral IGBTs are also plotted. The MOSFET fabricated in this letter demonstrates the highest figure-of-merit of 62 MW/cm^2 among any lateral MOSFETs ever reported, which is more than ten times better than the "Si limit."

on-resistance is as low as 30 mΩ · cm^2, and the MOSFET broke down at the gate oxide when a drain voltage of 1100 V was applied (not shown). The 4H-SiC $(000\bar{1})$ face is effective in enhancing the MOSFET performance.

Fig. 5 shows the relationship between breakdown voltage and on-resistance for major lateral SiC MOSFETs reported in the literature and this letter. For comparison, the relationship for Si lateral superjunction MOSFETs [17] and Si lateral IGBTs [18], [19] are also represented in Fig. 5. In the case of lateral MOSFETs, the figure-of-merit had not been able to exceed 45 MW/cm^2. The figure-of-merit obtained in this letter is 62 MW/cm^2 for the two-zone double-RESURF MOSFET on the 4H-SiC $(000\bar{1})$ face (1580 V–40 mΩ · cm^2), which is more than ten times better than the conventional "Si limit."

IV. Conclusion

The authors have fabricated the double-RESURF MOSFETs on the 4H-SiC $(000\bar{1})$ face. The MOSFETs with N_2O-grown oxides on $(000\bar{1})$ showed a high channel mobility of 32–36 cm^2/V · s. The fabricated MOSFETs with a short drift length of 10 μm and a long drift length of 20 μm broke down at the gate oxides and in SiC, respectively. The increase of RESURF doses improves the blocking characteristics (higher breakdown voltage), as well as the ON-state characteristics (lower on-resistance), in the MOSFETs with a long drift region. In the MOSFET with a long drift region, the breakdown voltage at zero gate bias reached 1580 V, and the on-resistance was as low as 40 mΩ · cm^2. The increase of channel mobility leads to lower channel resistance. The figure-of-merit of the fabricated MOSFET on the $(000\bar{1})$ face was as high as 62 MW/cm^2, which is more than ten times higher than the "Si limit."

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